CMP 334 Syllabus Fall 2017

1. Course Description

Introduction to digital logic-expressions, gates, flip-flops, adders. buses, multiplexers

Introduction to assembly language and assembly level organization - data representation, instruction formats, addressing modes, interrupts.

Memory systems-caches (mapping and management policies) and memory hierarchies, latency and bandwidth, virtual memory (page tables, TLB).

Input/Output- buses, channels and DMA.

Performance considerations- pipelining, RISC architecture, branch prediction, introduction to instruction level parallelism.

Credits: 4 *(expect to 12 hours a week on this material outside of class)*

Prerequisites: 167CMP , CMP 232 or departmental permission.

2. Instructor: Bowen Alpern

email: Bowen.Alpern@lehman.cuny.edu

office: GI 137 A

hours: M 5 to 6 pm, W 1 to 2 pm, and by appointment

3. Sections

CMP 344–I401 M W 11:00 pm – 12:40 pm Gillet 231
CMP 334-ZH01 M W 7:40 pm – 9:30 pm Gillet 231

If you wish to attend the other section from which you were assigned on a regular basis, please let me know about it. It should be fine for you to attend it only once or twice, provided there is available seating.

4. Learning Objectives

At the end of this course students will be able to:

- Understand how basic processor components such as flip/flops, registers, buses, adders, clocks, and control logic are built from digital logic.
- Do a comparison of instruction sets and the architectures of RISC, CISC, and Stack computers.
- Understand computer pipelining including the performance benefits and hazards; and the hardware and software techniques used to minimize the negative impacts of the hazards.
- Use Amdahl's law and the computer performance equation to predict the impact of changes to hardware configurations such as faster clocks, better floating-point units etc.
- Understand the memory hierarchy and the impact of various cache organizations. Be able to predict the performance of memory hierarchy changes.
- Understand the implications of todays multi-core processor chips including synchronization and memory consistency

5. Textbook

Computer Organization and Design: *The Hardware / Software Interface*

Hennessy and Patterson
ISBN: 978-0-12-801733-3
Online material: http://booksite.elsevier.com/9780128017333/
limited preview (chapters 1 and 2)

I will be using the ARM Edition. There are many.. Any from the third edition on should work nearly as well. The is a copy on reserve in the library, if you need to sync up. Some are available on the internet, but before the fifth editions, "The Basics of Logic Design" was on a CD and may not be included with the pdf. I will rely on your having access to this appendix!

Other texts

Computer Organization and Architecture - Null and Lobur
Computer Organization and Architecture - Stalling

6. Grading Policy

20% First in class exam *

20% Second in class exam *

20% Final exam, part 1

20% Final exam, part 2 *

10% Quizzes

10% Homework

All quizzes and exams will be closed book. No electronic devises will be allowed as well. You may bring one 8½ x 11 piece of paper with notes on either side to exams. Your notes must be in your own hand writing (but no magnifying devices will be allowed). Fold and turn in your "cheat sheet" with your exam.

* The material covered on the second part of the final will be the same as that covered by the in class exams. If your score is better on this part of the final than on one or both of the in class, I will devalue the latter (to 15%) and increase the value of that part of the final accordingly.

Please speak with me if you think you might be unable to take one of the in class exams. A (slightly more difficult) make-up exam will be given during finals week.

Homework and quizzes will be an important part of the course. I expect to give a lot of each. There will be no makeup quizzes and homework after I go over it in class (or post a solution on Blackboard) will not be accepted. Otherwise, late homework will receive half credit. I will ignore a few of your lowest scores on these in computing your class grade. I intend to post solutions both to homework and to quizzes on Blackboard.

Homework is an important component of your overall grade. Do not neglect it! Assignments will *generally* be due the midnight preceeding the

second class after it was assigned. (Use the intervening class to make sure that you are clear about what is being asked of you.)

Homework will ***only*** be accepted through Blackboard. Where possible, answer the question in the text of your submission. If it is more convenient for you to include an attachment, I prefer that they be in pdf, Microsoft Office, or some open source Office format. If you must attach a photo of your work make sure it is legible! (Write clearly in dark ink on white paper, preferably unlined. Light the page well. Take the photo straight on, rather than at an angle. Before attaching, review it to make sure that you can read it easily.) Attachments that I find difficult to decipher will receive reduced scores.

The purpose of a homework assignment is to have you engage meaningfully with the problem so that, after I present a solution in class, you would be able to answer a similar problem (should it appear on an exam, for example). Submit your best work even if you know it is not entirely correct. My grading of homework will be perfunctory: 2 points if your answer is substantially correct, 1 if it is incorrect but reflects a credible effort, 0 if you are way off or did not submit a solution.

If you have a question or disagree with the grade I have given you on an assignment, quiz, or exam, please take it up with me either by email or in my office. See me, if you don't understand something, have questions, or feel you are falling behind. I only expect to be on campus Mondays and Wednesdays. I will be around and usually in my office between my classes and I can arrange to come in early or stay late if that is what works for you.

My exams tend to be overly difficult. Do not let that discourage you! I expect to grade the class on a B- curve (there will be as many grades B or above as C+ or below).

There is an anomaly in Lehman's grading system that occasionally makes it to a students advantage to fail a class rather that pass it with a low grade. If you feel that you might be in that rare situation, let me know the minimum passing grade you would want for the course (and check back later to make sure that I have taken note of it).

7. Attendance and Punctuality

There is an **attendance requirement** at Lehman College. Students with poor attendance and/or repeated lateness (no matter what the reason) will have their grades reduced. If I forget to pass our an attendance sheet, please start one for me.

If an emergency prevents you from attending class, it is your responsibility to obtain notes from a classmate and study them for understanding. It is a wise move to get a buddy.

It can be disruptive to have several students arrive late to class. Please try to be on time! If you arrive close to the beginning of class and the door is closed, wait until I ladmit latecomers ten minutes into class. If you are more than 15 minutes Llate, knock quietly and someone will let you in.

8. Accommodating Disabilities

Lehman College is committed to providing access to all programs and curricula to all students. Students with disabilities who may need classroom accommodations are encouraged to register with the Office of Student Disability Services, Shuster Hall, Room 238, phone number, 718-960-8441. Contact the office for more information.

9. Tentative Schedule

8/28 8/30	Basic computer model Basic processor model, Boolean algebra
9/ 4 9/ 6	Labor Day Performance, Truth tables, the tiny processor
9/11 9/13	Amdahl's law, execution, instructions compilation, gates Performance examples, straight line code, decoder/multiplexer
9/18 9/20	ISA types, half & full adder, negative numbers, Rosh Hashanah
9/25 9/27	Comparisons, flow charts, ripple-carry adder, computer arithmetic The ALU, Fast multiplication, floating point numbers
10/ 2 10/ 4	Lookahead-carry adders, memory (R/S flip-flop) **Exam 1**
10/ 9 10/11	Columbus Day Sequential logic, clocks, latches and flip-flops
10/16 10/18	Kinds of flip-flop, counters, registers and register files Instruction execution, abstract pipelining
10/23 10/25	Up from the basic processor model, pipeline preview Single cycle implementation, perfect pipeline
10/30 11/ 1	5-stage implementation, interstage registers, performance Hazards: structural, data, control, bubbles in the pipe
11/ 6 11/ 8	Data hazards, forwarding, performance Control hazards , branch prediction, performance
11/13 11/15	Exceptions, instruction level parallelism, super-scalar **Exam 2**
11/20 11/22	Simple cache, locality principle, performance Multilevel caches, performance, memory hierarchy
11/27 11/29	Disk I/O, disk performance Virtual memory, TLB, performance
12/ 4 12/ 6	Parallelism 1, ILP, Flynn taxonomy, clusters, etc. Parallelism 2, the Parallel Memory Hierarchy model
12/11 12/13	Review Reading day
12/18 12/20	**Final Week**